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Wafer Carriers (Boats)

Just a Rack—or the Key to Semiconductor Process Success?

MakeCoTech Engineering Insights | Issue 01:
July 2026

Wafer Carriers (Boats): Just a Rack—or the Key to Semiconductor Process Success?

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How wafer carrier design influences thermal uniformity (400–1250°C), mechanical integrity, slip-line formation, particle generation, contamination control, process stability, and ultimately manufacturing yield.

The primary objective of Chemical Vapor Deposition (CVD) and Atomic Layer Deposition (ALD) is to deposit high-quality semiconductor and functional thin films onto substrates such as silicon wafers. Whether using a single-wafer pedestal or a batch wafer carrier (boat), the wafer support forms the critical interface between the wafer and the process environment, directly influencing heat transfer, gas flow, deposition uniformity, and overall process performance.

The primary function of a wafer carrier (or wafer boat) is to securely support and position semiconductor wafers inside the process reactor throughout the thermal cycle. At first glance, it may appear to be nothing more than a simple rack. However, its design has a direct impact on manufacturing productivity. The more wafers that can be reliably accommodated within the fixed volume of a reactor—without compromising process performance or wafer quality—the higher the throughput and overall production efficiency. Although this discussion primarily focuses on silicon wafers, wafer carriers are also used for other substrate materials and process applications, including silicon carbide (SiC), sapphire, glass, quartz, boron nitride, and alumina. The engineering principles discussed here remain broadly applicable across these material systems.

Excessive stresses can initiate slip-line formation, and ultimately compromise device yield.

Slip-Line Formation & Overlay Error

Silicon Wafer behavior on the support points:

Silicon wafers are thin discs (typically around **0.7 mm** thick for 300 mm wafers) sliced from single-crystal silicon ingots. Although silicon is a stiff material, wafers are far from rigid because of their large diameter-to-thickness ratio. Once placed on the carrier support slots, they naturally deform under their own weight. The resulting deflected shape is highly curved and resembles the deformation of a Pringles® potato chip, although at a much smaller scale. If the support geometry is not properly optimized, this deformation creates localized stress concentrations at the contact points. Excessive stresses can initiate slip-line formation, increase wafer warpage, and ultimately compromise device yield. Once formed, slip-line defects are permanent crystallographic defects and cannot be removed during subsequent process steps.

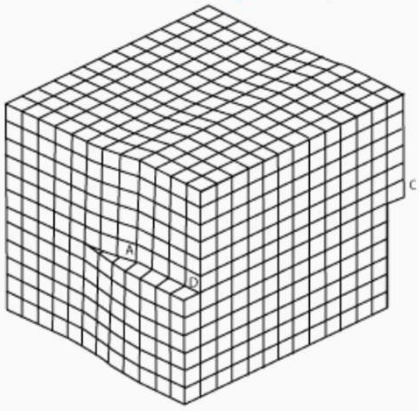
Wafer Slip-Line Control: A Hidden Design Requirement

At MakeCoTech, we support semiconductor equipment manufacturers in developing wafer carrier designs for demanding thermal processes, typically ranging from 900°C to 1250°C. Our engineering approach combines advanced thermo-mechanical simulation, in-depth understanding of silicon material behavior, contact mechanics, and thermal expansion analysis to minimize both gravitational and thermally induced slip-line formation while maintaining the required process throughput. We also provide guidance on manufacturing tolerances to ensure that the final carrier performs in production as intended—**not only in simulation.**

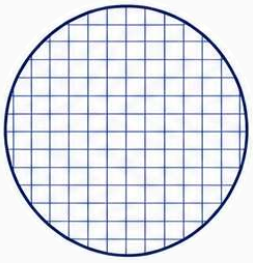
Slip/Overlay

Slip-lines generated by thermally and mechanically induced stresses distort the silicon crystal lattice, resulting in wafer deformation and lithography overlay errors.

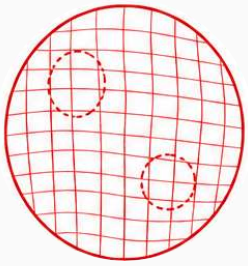
Screw dislocation (slip-line) in crystal lattice



Ideal wafer (No Slip-line)



Uniform wafer shape → accurate pattern alignment



Wafer deformation → pattern misalignment (overlay error)

MakeCoTech supports in developing wafer carrier designs for demanding thermal processes **free from slip-lines** ranging from 900°C to 1250°C.

Carrier Material Choices & Particles

Carrier Material choices

Selecting the appropriate material for a wafer carrier is a critical engineering decision. The optimum choice depends on process chemistry, operating temperature, particle performance, mechanical stability, preventive maintenance (PM) interval, and total cost of ownership. There is no universal solution—every semiconductor process has its own requirements.

Common carrier materials include:

- Quartz (various surface finishes)
- Silicon (single-crystal and polycrystalline)
- Silicon carbide (CVD-coated or uncoated)
- Graphite (various coatings)
- Alumina

Each material offers unique advantages in thermal performance, chemical compatibility, particle performance, mechanical integrity, lifetime, and cost.

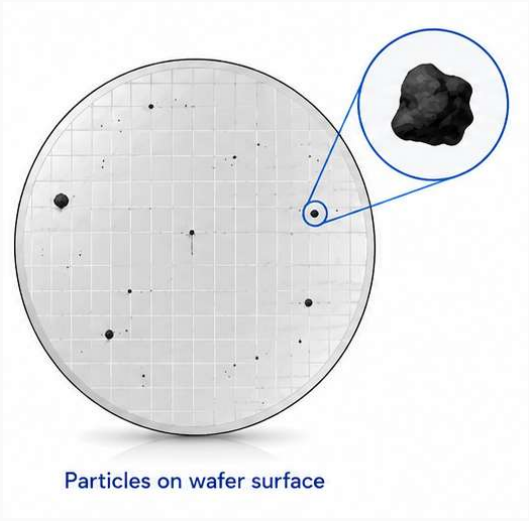
Particles: A Silent Yield Killer!

Major particle sources include:

- Backside scratches from wafer/carrier contact in thermal cycles.
- Vibration during processing or transport
- Material degradation at elevated temperatures and etching
- Gas-phase reactions and process deposits
- Thin-film cracking by thermal mismatch (CTE) between deposited film and substrate, triggered by intrinsic stress in the film.

This topic deserves a dedicated discussion and will be covered in a future issue of MakeCoTech Engineering Insights.

Even microscopic particles can create critical defects on active device areas, leading to electrical failures, yield loss, and reduced long-term reliability. As semiconductor technology continues to scale, particle specifications become increasingly stringent, making particle control one of the most important design requirements for wafer carrier engineering.



Consequence of particles

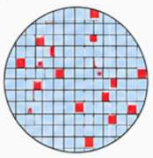
1 Defects in critical layers

Particles introduce defects in thin films and interfaces that cannot be removed in later process steps

2 Electrical failure

Defects caused by particles can lead to opens, shorts, or increased leakage, resulting in electrical failure

3 Yield loss



More defective dies per wafer directly reduce overall yield and increase manufacturing cost.

Controlling Particle Generation & Structural Integrity at High Temperatures

Controlling Particle Generation

One of the most important objectives in wafer carrier design is minimizing particle generation. A major source of particles originates from backside scratches caused by the interaction between the wafer and its support slots.

During thermal processing, differences in the coefficient of thermal expansion (CTE) between the wafer and the carrier produce relative sliding at the contact points. Depending on the carrier material, slot geometry, thermal gradients, and surface finish, this sliding may generate abrasive wear on either the wafer backside or the carrier itself, leading to particle generation.

From an engineering perspective, backside scratches are primarily governed by three design parameters:

Backside Scratches

= Contact Pressure *(Slot Geometry)*

× Relative Sliding *(Material Selection & Thermal Gradients)*

× Surface Morphology *(Surface Finish*

Reducing any of these factors helps minimize particle generation, improve wafer quality, and extend carrier lifetime.

Backside Scratches:
Contact Pressure (Slot Geometry Design)
× Relative Sliding During Thermal Expansion (Material Selection & Thermal Gradients)
× Surface Morphology (Surface Finish)

Progressive creep deformation reduces wafer positioning accuracy and ultimately requires carrier replacement

Other Sources of Particles

Additional particles may originate from:

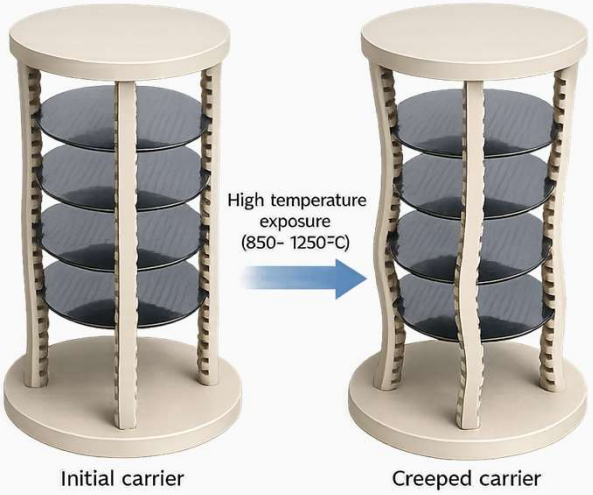
•Carrier vibration during processing or transportation. In this case carrier stiffening be considered which needs to be engineered according to target requirements and process sensitivity analysis.

•Material degradation at elevated temperatures

•Gas-phase reactions and process deposits

These sources can often be reduced through optimized carrier design, including improved structural stiffness, optimized support geometry, and appropriate support configurations.

If your process is limited by particle-related yield loss, a detailed engineering assessment of the wafer carrier often identifies practical opportunities to improve particle performance and manufacturing yield.



Structural Integrity at High Temperatures

Wafer carriers often support significant payloads while operating at temperatures approaching 1200°C. Under these demanding conditions, structural integrity becomes a critical design requirement.

The principal failure mechanisms include:

•**High-temperature creep and buckling**, resulting in gradual deformation and loss of wafer positioning accuracy.

•**Thermally induced stresses** generated during furnace loading and unloading, when large thermal gradients develop while the reactor remains at elevated temperature.

•**Mechanical loads during transport and maintenance**, as fully loaded carriers are frequently handled outside the reactor during service operations.
A robust carrier design must maintain **dimensional stability, mechanical integrity, and process repeatability** throughout its operational lifetime

The Carrier Should Be "Invisible" to the Process

Beyond mechanical integrity, an effective wafer carrier should interfere as little as possible with the deposition process itself. Ideally, the support rods and wafer slots should be **almost invisible to the process gas**. Oversized or excessively massive support structures locally modify the gas flow and the surface-to-volume ratio around the wafer edge, which can alter precursor transport and reaction kinetics. The result may be local variations in deposition rate, film thickness, or within-wafer uniformity.

Consequently, wafer carrier design is always a compromise between **mechanical stiffness, thermal performance, particle control, and minimal process interference**.

Closing

Whether you are developing a new wafer carrier or improving an existing design, MakeCoTech provides engineering support in thermo-mechanical analysis, particle reduction, slip-line control, structural integrity, and process optimization to improve manufacturing yield.

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Kianoosh has more than 18 years of experience in advanced engineering, finite element analysis, and product development across the semiconductor, automotive, and research industries. His expertise spans semiconductor equipment, finite element analysis, nonlinear material modelling, contact mechanics, thermo-mechanical simulations, and wafer carrier optimization. He enjoys helping companies transform complex engineering challenges into robust, manufacturable solutions.

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